REMARKS/ARGUMENTS

Claims 1-18 were pending in the present application. By virtue of this response, no claims have been cancelled, no claims have been amended, and no new claims have been added. Accordingly, claims 1-18 are currently under consideration. Amendment and cancellation of certain claims is not to be construed as a dedication to the public of any of the subject matter of the claims as previously presented. No new matter has been added.

Rejections under 35 U.S.C. §102(b)

The Office has rejected claims 1, 3, 5-6, 8, 10-11, 13-14, and 16-17 as allegedly being anticipated by Hatano et al. (5,432,808). As discussed in detail below, it is respectfully submitted that these rejection claims are not anticipated by Hatano and that, as a result, the anticipation rejection should be withdrawn.

The rejection of most of these claims as being anticipated by Hatano is not new. (The rejection of claim 5, previously indicated as including allowable subject matter, is new.) Taking claim 1 first, in response to the previous office action, Applicant amended claim 1 to include a recitation of "said semiconductor light-emitting device chip is connected to the mount surface of said mount member by solder between the semiconductor light-emitting device chip and said mount surface of said mount member, with said stack facing said mount surface."

The Examiner contends that in the present office action Hatano discloses the "solder" feature. Applicant respectfully disagrees. The Examiner points to col. 10, line 30 of Hatano as disclosing this feature. Specifically, the Examiner appears to be contending that the recitation of "die bonding" at col. 10, line 30 of Hatano discloses the "solder" feature. See the section of the Office Action entitled "Response to Arguments." However, the Examiner's contentions are not completely clear as the Examiner seems to contend that the cited section of Hatano discloses all of "solder, cladding, die bonding, and not just solder."

In any event, the cited section of Hatano does not disclose "solder". Applicant respectfully reminds the Examiner that, in order for a reference to be anticipatory, the reference must disclose all of the claim features.

In the first place, while it does not appear relevant, the cited portion of Hatano does not disclose "die bonding" at all. The cited portion does disclose that a cladding layer 43 is formed on a buffer layer 42. Furthermore, not only is there discussion of "die bonding," neither is there discussion of "solder." If the Examiner continues to contend that Hatano discloses the "solder" feature, the Applicant respectfully requests the Examiner to cite to a particular column and line of the Hatano reference that is considered to disclose this feature. Since the Examiner's citations (and paraphrases thereof) are somewhat ambiguous, it would be helpful if the Examiner provided an exact quote of the cited portion in the Office Action so that Applicant can be certain to what language the Examiner is referring.

Without limiting the claims beyond what is recited in them, Applicant notes that, in accordance with the structure of claim 1, a group of components to be placed at an upper level of the claimed device may be produced "in advance" and connected to the mount member via solder. If Hatano can be considered to disclose corresponding layers, those layers are apparently produced through epitaxial growth upon the "mount member" (assuming Hatano even discloses a "mount member") and there is no solder between a mount surface and a light emitting device chip.

Perhaps the Examiner considers the "solder" feature to be inherent. However, a feature is inherent in a prior art reference only if the prior art necessarily functions in accordance with, or includes, the claimed limitation. As just discussed, since the layers may be produced through epitaxial growth on the "mount surface," the Hatano device does not necessarily include the "solder" feature. As a result, the "solder" feature is not inherent.

With specific regard to claim 10, the Examiner has not even addressed where Hatano is alleged to disclose "said stack is formed by stacking the semiconductor layers on the surface of said chip substrate in advance of connecting said semiconductor light-emitting device chip to the mount

surface of said mount member." It is respectfully submitted that, in any event, Hatano fails to disclose this feature.

Thus, the anticipation rejection is improper and should be withdrawn.

Rejections under 35 U.S.C. §103(a)

The Office has rejected claim 2 as allegedly being obvious over Hatano et al. (5,432,808). As discussed below, it is respectfully submitted that Hatano does not render the subject matter of claim 2 obvious.

In the first place, as has been discussed above with regard to the anticipation rejection, Hatano fails to disclose a "solder" feature. For at least this reason alone, the obviousness rejection must fail.

Furthermore, even if Hatano could be said to disclose the "solder" feature, the Examiner has failed to meet the burden for setting forth a prima facie case of obviousness. That is, the Examiner is relying on a proposed modification to a reference, where the reference itself admittedly does not include a feature of the claim -- "said mount surface is curved to protrude . . . ." However, the Examiner must cite a suggestion in the reference or in knowledge known to one of ordinary skill in the art to make the modification. Merely asserting that the feature is "well known" is not sufficient. Perhaps a contention of design choice (which is essentially what the Examiner is contending) would be appropriate if the various "choices" were well-known to be interchangeable, and the Examiner provided evidence that the choices were well-known to be interchangeable. Here, the Examiner merely asserts in a very conclusory manner that "any of these method are well accepted practice . . ." The Examiner has cited nothing to support the assertion that any of these methods are well accepted practice," let alone an assertion (not made) that it is well known that these methods are interchangeable.

Thus, since Hatano does not disclose the "solder feature," and since the Examiner has otherwise failed to set forth a proper prima facie case of obviousness, the obviousness rejection is improper and should be withdrawn.

Allowable Subject Matter

Claims 4, 7, 9, 12, 15 and 18 are objected to as being dependent upon a rejected base.

Applicant appreciates the Examiner's indication that these claims recite allowable subject matter. Applicant believes that the base and intervening claims are allowable. Applicant has thus not rewritten the claims at this time.

CONCLUSION

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue. If it is determined that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the event the U.S. Patent and Trademark Office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing docket no. 245402004500. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Dated: October 30, 2003

Respectfully submitted,

By_____

Alan S. Hodes
Registration No.: 38,185
MORRISON & FOERSTER LLP
755 Page Mill Road
Palo Alto, California 94304
(650) 813-5622